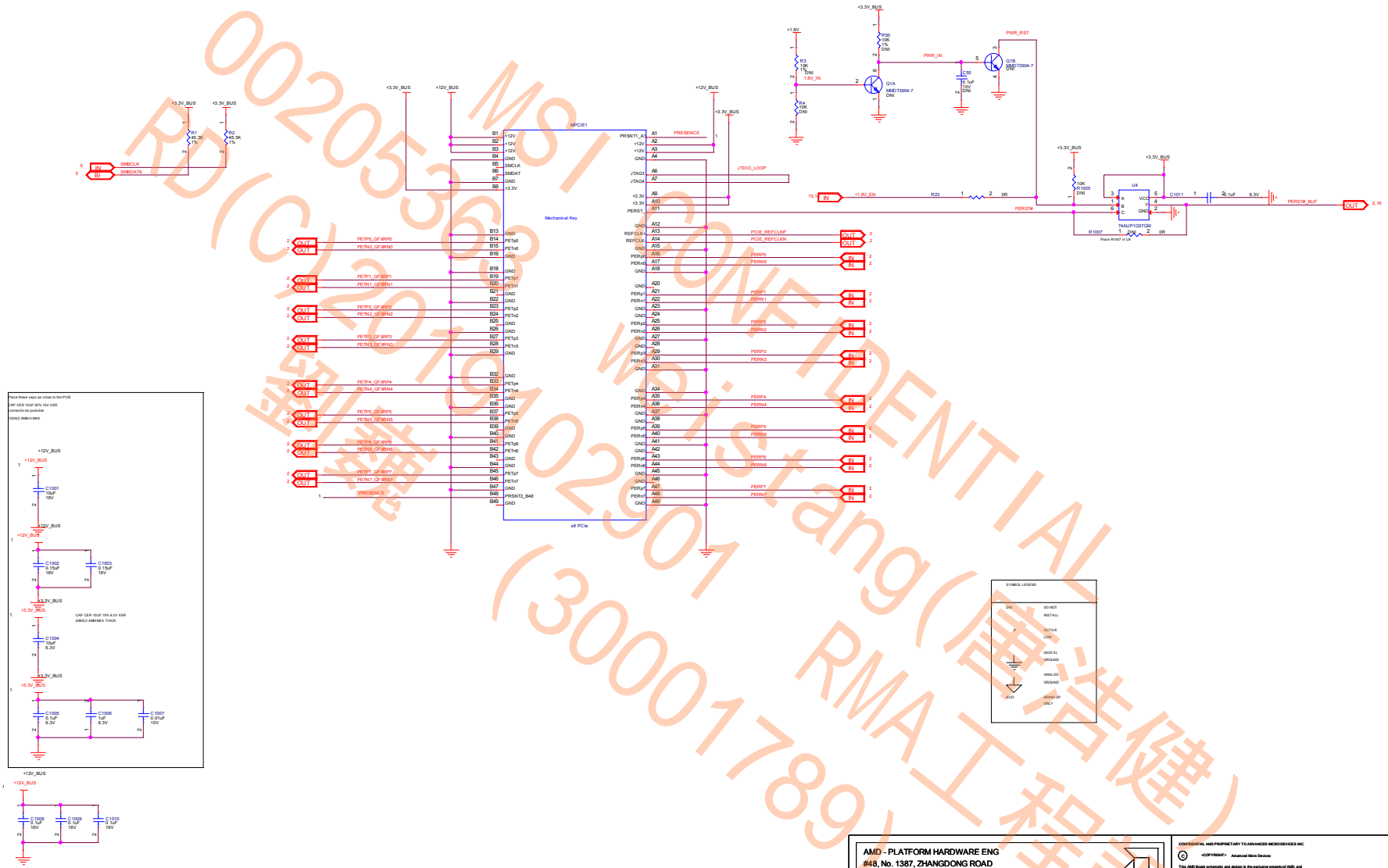


PCI-EXPRESS EDGE CONNECTOR

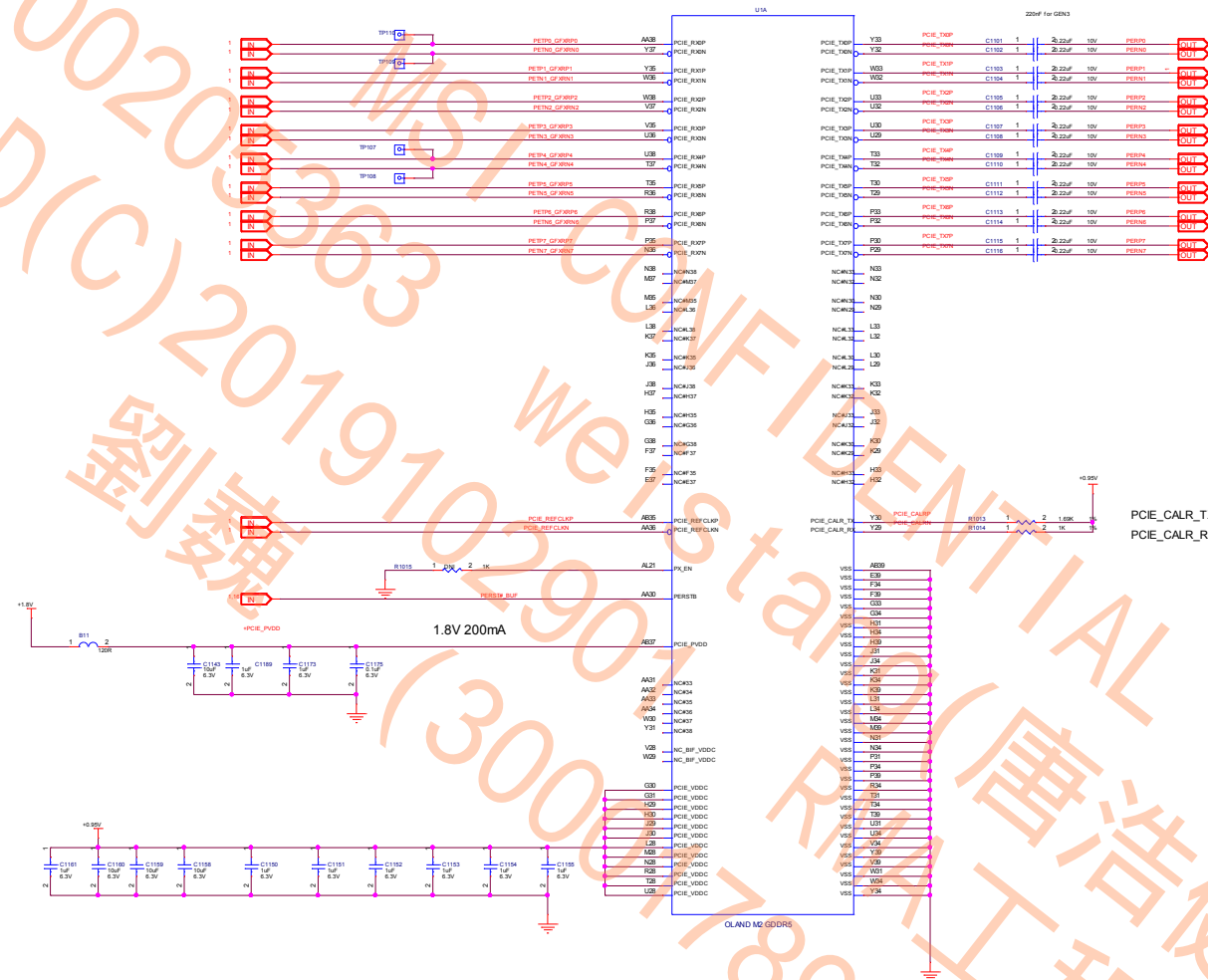


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|---|--|---|--|
| AMD - PLATFORM HARDWARE ENG #49, No. 1367, ZHANGDONG ROAD SHANGHAI, CHINA 201203 | | | |
| SHEET: PCIE Edge Connector | | REV: 2.0 | |
| DATE: Tue Sep 22 06:34:19 2015 | | SHEET NUMBER: 1 OF 20 | |
| DOCUMENT NUMBER: 105-C869w-008 | | TITLE: Oland G5 2GB VGA/SDVI/HDMI/DP | |


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Oland PCIe Interface

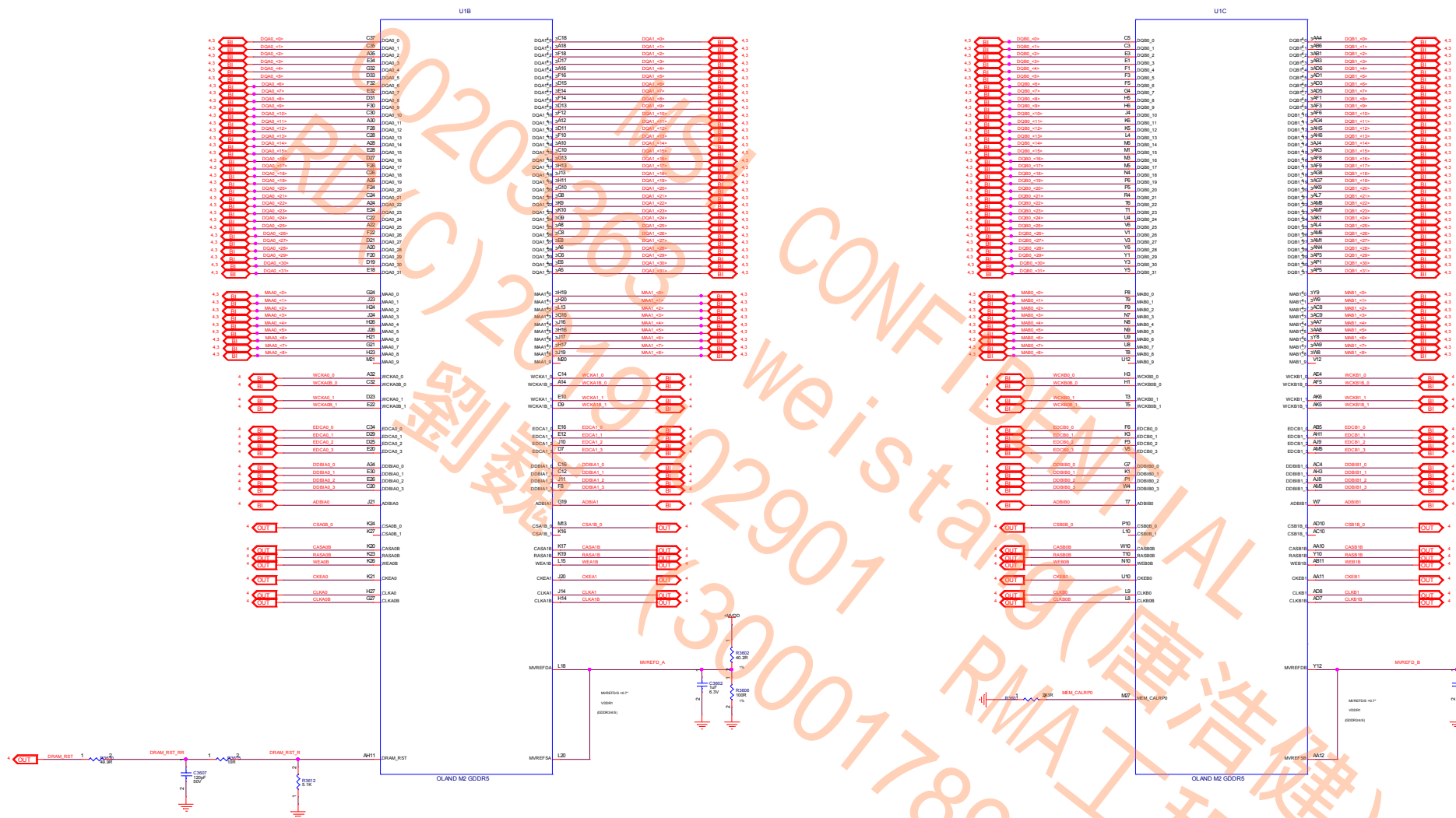
NOTE: Some of the PCIe testpoints will be available through vias on traces.



PCIE_CALR_TX 1.69k pull up for Oland
PCIE_CALR_RX 1k pull up for Oland

| | |
|--|--|
| <p>AMD - PLATFORM HARDWARE ENG #48, No. 1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203</p> | <div style="text-align: center;">  </div> |
| <p>SHEET: Clamd PCIe Interface</p> | <p>CONFIDENTIAL AND PROPRIETARY TRY TO ADVANCE MICRODEVICES INC. ©COPYRIGHT: Advanced Micro Devices</p> <p><small>This AMD/BSI schematic and design is the exclusive property of AMD, and is provided only as a reference under a non-disclosure Agreement with AMD to qualified personnel. Further distribution or disclosure is strictly prohibited. Use of this information and design for any purpose other than what is intended requires a signed Technology Content Agreement with AMD. AMD makes no representations or warranties of any kind regarding this schematic and design, including, but not limited to, any implied warranty of non-infringement or fitness for a particular purpose, and disclaims any responsibility for any consequences resulting from use of the information included herein.</small></p> |
| <p>DATE: Mon Sep 21 10:05:43 2015</p> | <p>REV: 2.0</p> |
| <p>SHEET NUMBER: 2 OF 20</p> | <p>TITLE:</p> <p style="text-align: right;">Clamd G5 2GB VGAs/DVI+HDMI/DP</p> |
| <p>DOCUMENT NUMBER: 105-C889xx-00B</p> | |

(3) Oland MEM Interface Ch A&B



AMD - PLATFORM HARDWARE ENG
#48, No. 1387, ZHANGDONG ROAD
SHANGHAI, CHINA 201203

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SHEET: Quad MEMORY INTERFACE

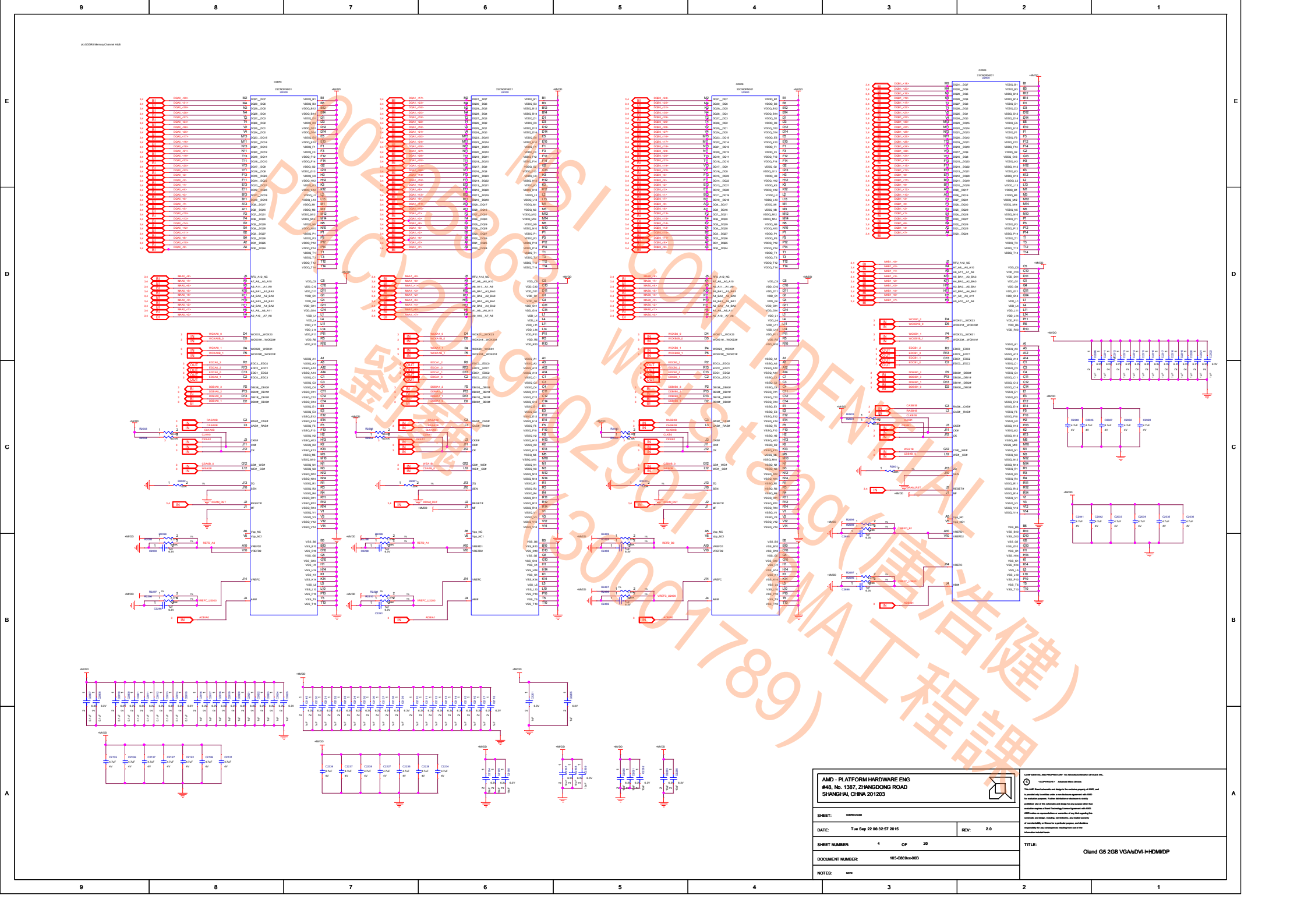
DATE: Mon Sep 21 10:05:45 2015

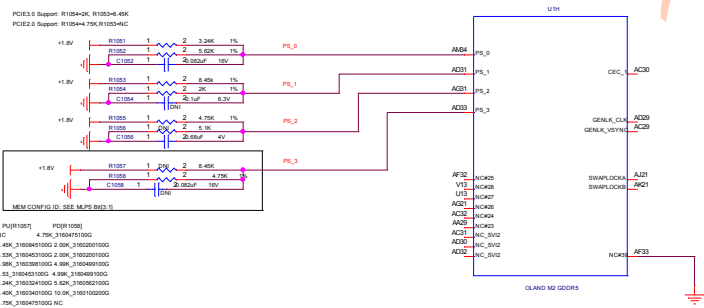
REV: 2.0


SHEET NUMBER: 3 OF 20

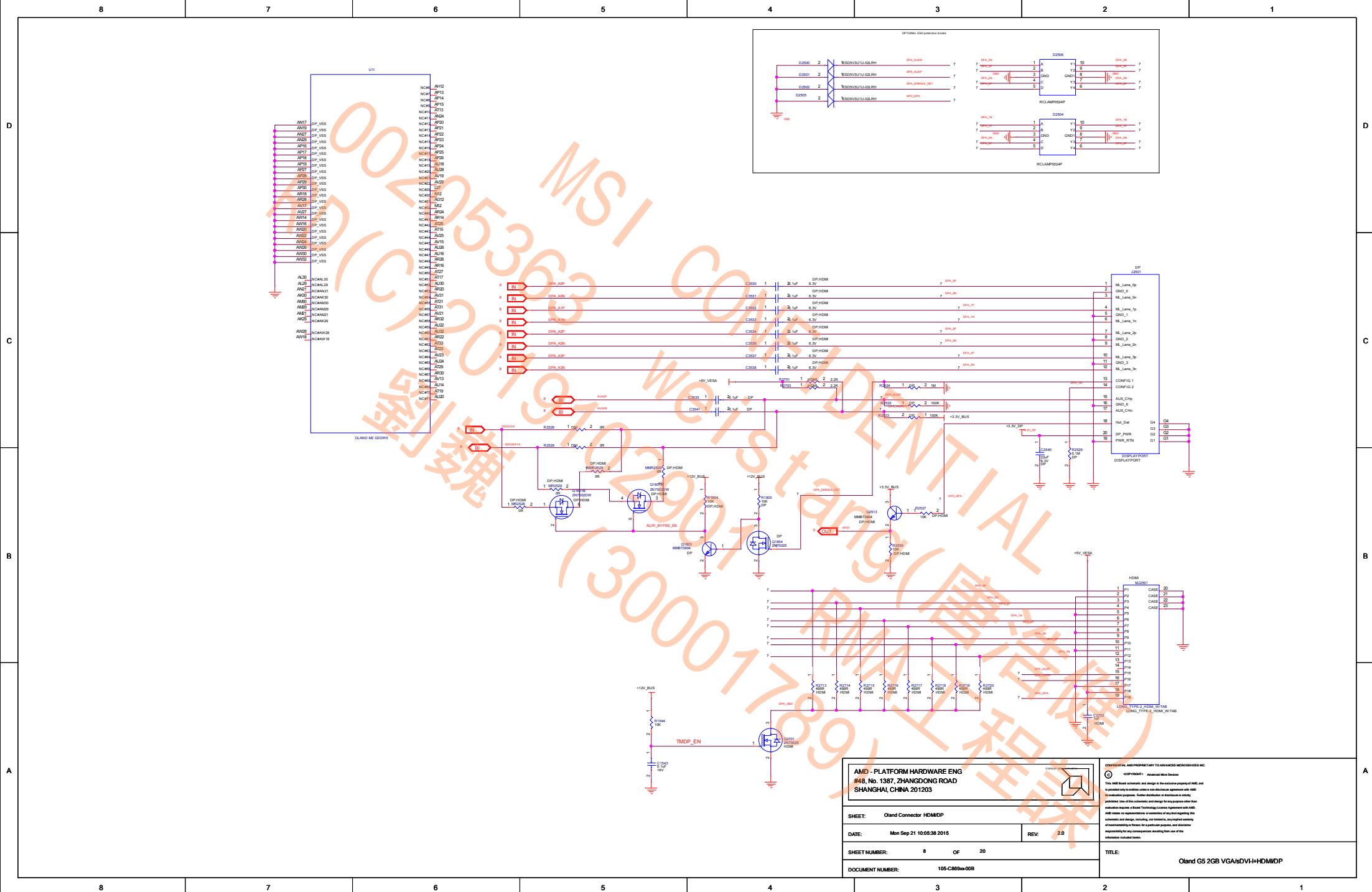
DOCUMENT NUMBER: 105-C869:xx-00B

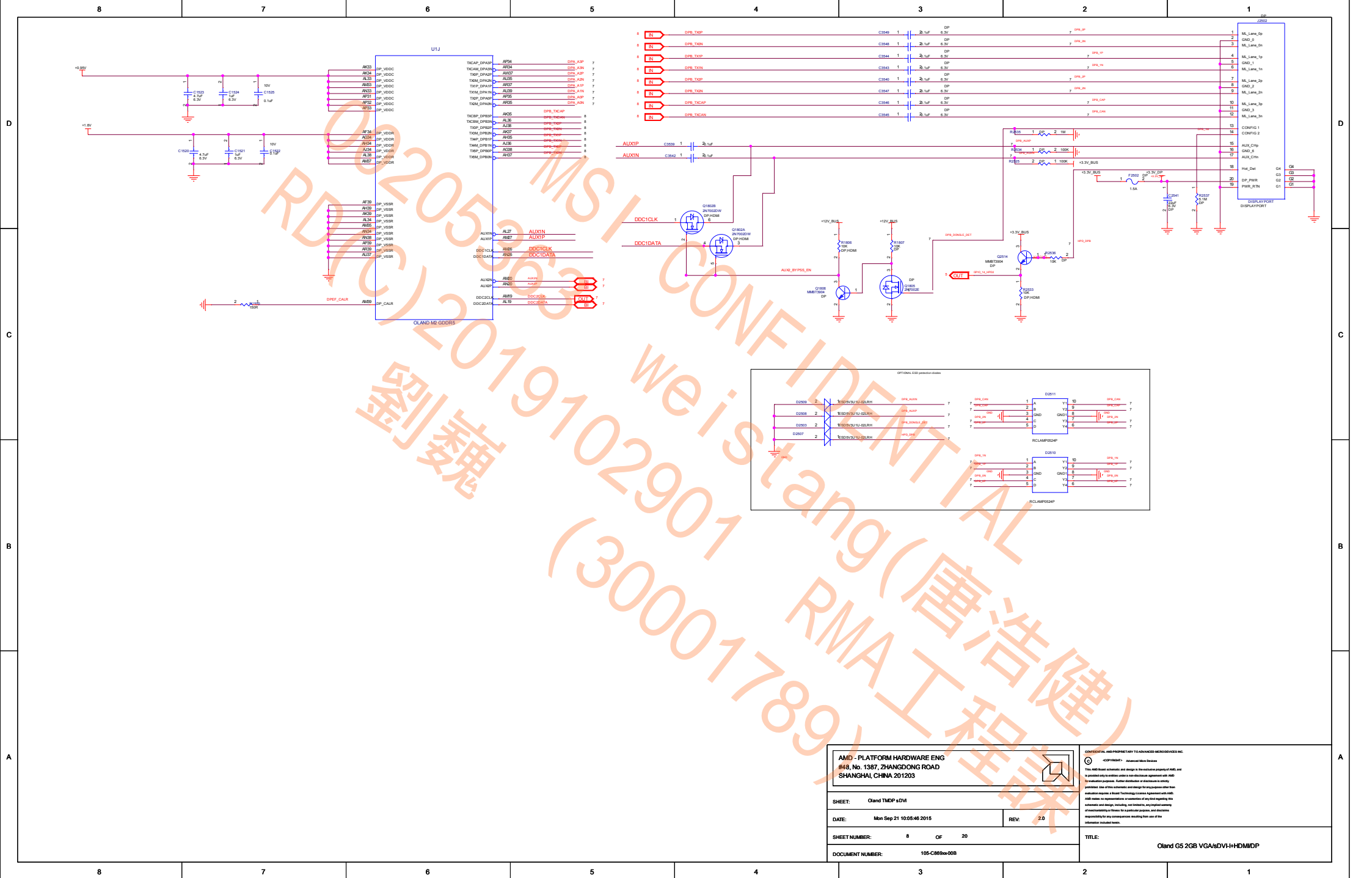
TITLE: Oland G5 2GB VGA/sDVI-I+HDMI/DP





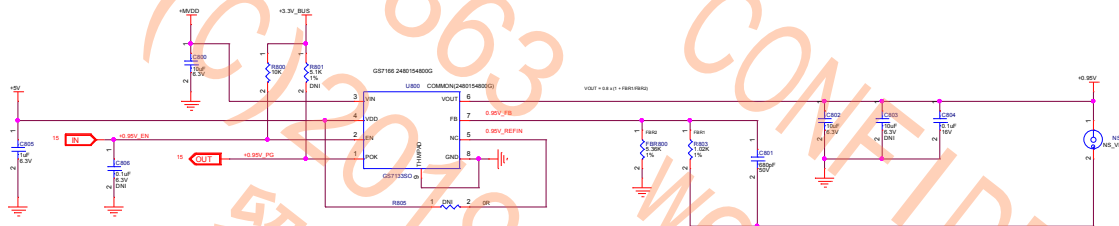
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|---|---|
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| <p>SHEET: Oland DAC and MLPS</p> |  |
| <p>DATE: Tue Sep 22 06:32:58 2015</p> | <p>REV: 2.6</p> |
| <p>SHEET NUMBER: 6 OF 20</p> | |
| <p>DOCUMENT NUMBER: 105-C869xx-00B</p> | |
| <p>NOTES: NOTE</p> | <p>TITLE:</p> <p style="text-align: center; font-weight: bold;">Oland G5 2GB VGA/sDV11+HDMI/DP</p> |





Linear Regulators

LDO #1: $V_{in} = +1.5V \pm 2\%$ $V_{out} = +0.95V \pm 2\%$ $I_{out} = 1.44A (TYP) RMS MAX$
PCB: 50 to 70mm sq, copper area for cooling

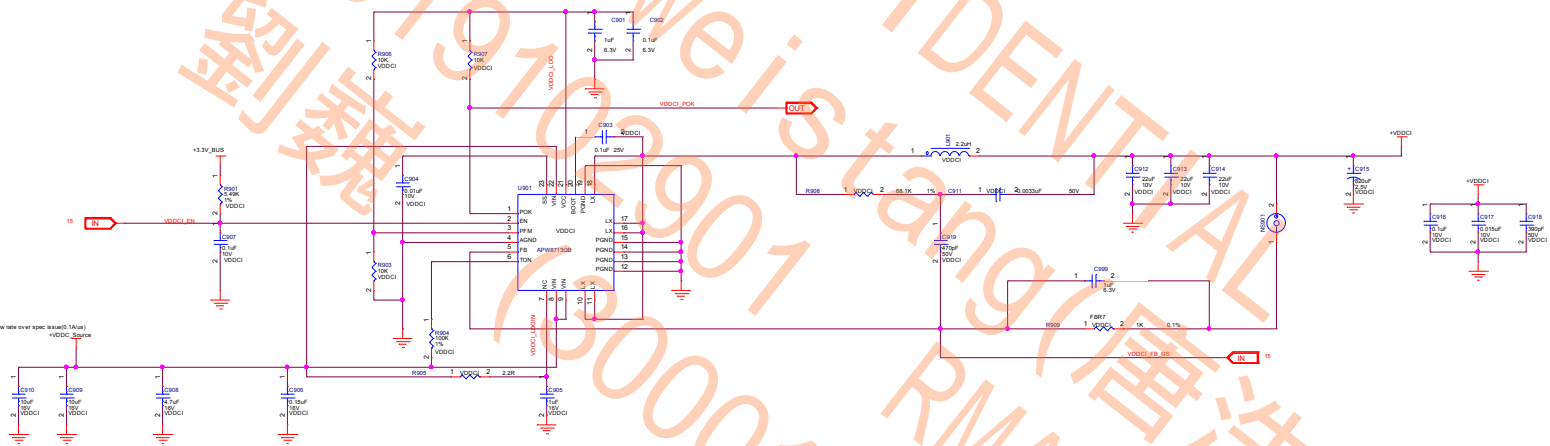


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|--|----------|
| AMD - PLATFORM HARDWARE ENG #49, No. 1367, ZHANGDONG ROAD SHANGHAI, CHINA 201203 | |
| SHEET: 0.95V | |
| DATE: Mon Sep 21 10:06:44 2015 | REV: 2.0 |
| SHEET NUMBER: 10 OF 20 | TITLE: |
| DOCUMENT NUMBER: 105-C869-008 | |

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| Oland G5 2GB VGA+DVI+HDMI+DP | |

Regulator for M10D

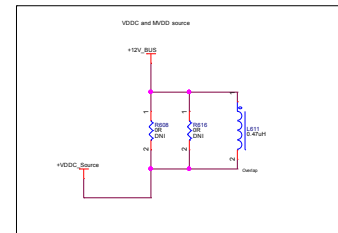
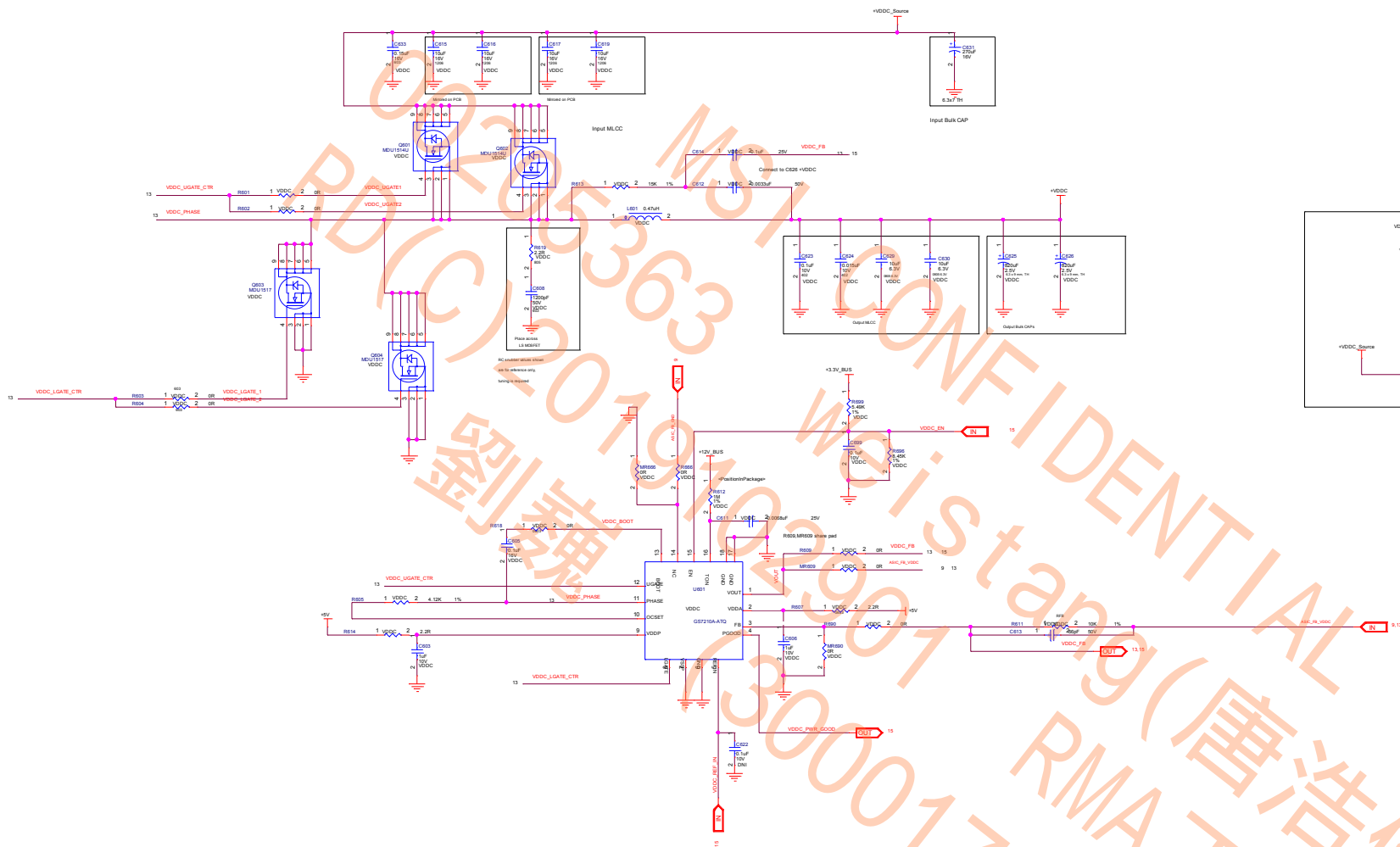
Use rVDDC_Source to share L801 to eliminate PCIe 12V current slew rate over spec issue(0.1A/us)
rVDDC_Source



| | | |
|--|--------------------------|----------|
| AMD - PLATFORM HARDWARE ENG #48, No. 1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203 | | |
| SHEET: | VDDC1 | |
| DATE: | Tue Sep 22 06:32:59 2015 | REV: 2.0 |
| SHEET NUMBER: | 12 | OF 20 |
| DOCUMENT NUMBER: | 105-C869x-008 | |
| NOTES: | NOTE | |

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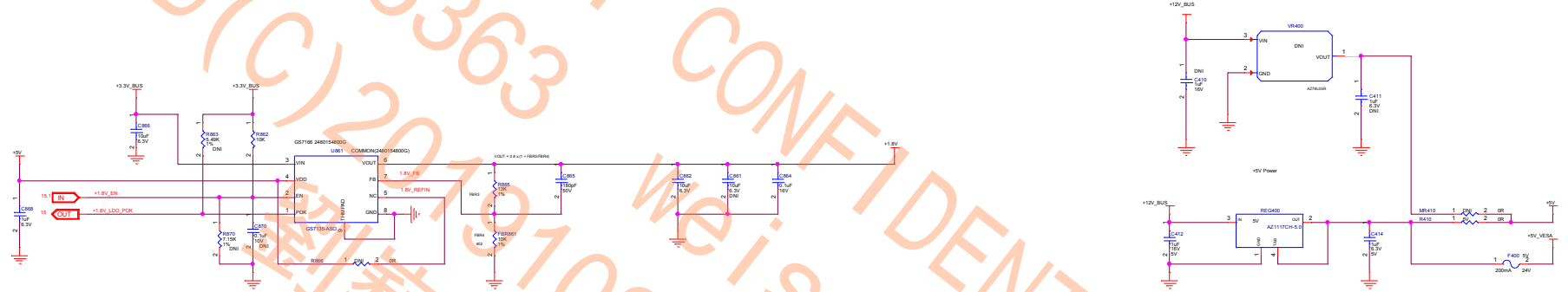
TITLE:
Oland G5 2GB VGA/sDVI-HDMI/DP



| | | | |
|--|--------------------------|---|------------------------------|
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| SHEET: | VDDC | REV: | 2.0 |
| DATE: | Mon Sep 21 10:06:41 2015 | | |
| SHEET NUMBER: | 13 OF 20 | TITLE: | Oland G5 2GB VGA+DVI+HDMI+DP |
| DOCUMENT NUMBER: | 105-C889-008 | | |

Linear Regulators


| | | | |
|---|--------------------------------------|-------------------------|---------------------------|
| LDO #2: | Vin = 3.00V to 3.60V (3.3V \pm 5%) | Vout = +1.8V \pm 1.2% | Iout = 1.5A (75V) RMS MAX |
| PCB: 50 to 70mm sq. copper area for cooling | | | |



| | |
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| AMD - PLATFORM HARDWARE ENG #49, No. 1367, ZHANGDONG ROAD SHANGHAI, CHINA 201203 | |
| SHEET: | Linear Regulators |
| DATE: | Mon Sep 21 10:06:44 2015 |
| REV: | 2.0 |
| SHEET NUMBER: | 14 OF 20 |
| DOCUMENT NUMBER: | 105-C869w-008 |

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| TITLE: | Oland G5 2GB VGA+DVI+HDMI+DP |

(19) Debug Circuits



L4 INNER
Different
Mem Clock
80 ohm +/- 10 %
5.12 mils / 7.48 mils

TITLE: Oland G5 2GB VGA/sDVI-I+HDMI/DP

| | | |
|------|------|---------|
| DW-L | HPD4 | DDCAUJM |
| HPD8 | HPD1 | DDCAUJ1 |
| DP | HPD3 | DDCAUJ8 |

| | | |
|--------|----------|----------|
| GPIO15 | VDDC_VDD | |
| GPIO25 | VDDC_VD1 | |
| GPIO7 | VDDC_VID | DEFAULT1 |
| GPIO5 | VR_HDT | |

12V_BUS
5.5A

MVDD SOURCE
1.5A

1.5V@10A

VDDCI SOURCE
0.6A

1.05V@6A

VDDC PHASE1 SOURCE
2.7A

VDDC@25A

VDDC PHASE2 SOURCE
2.7A

VDDC@25A

FAN
0.5A

0.95V SOURCE
1A

0.95V@1A

1.8V_LDO
0.5A

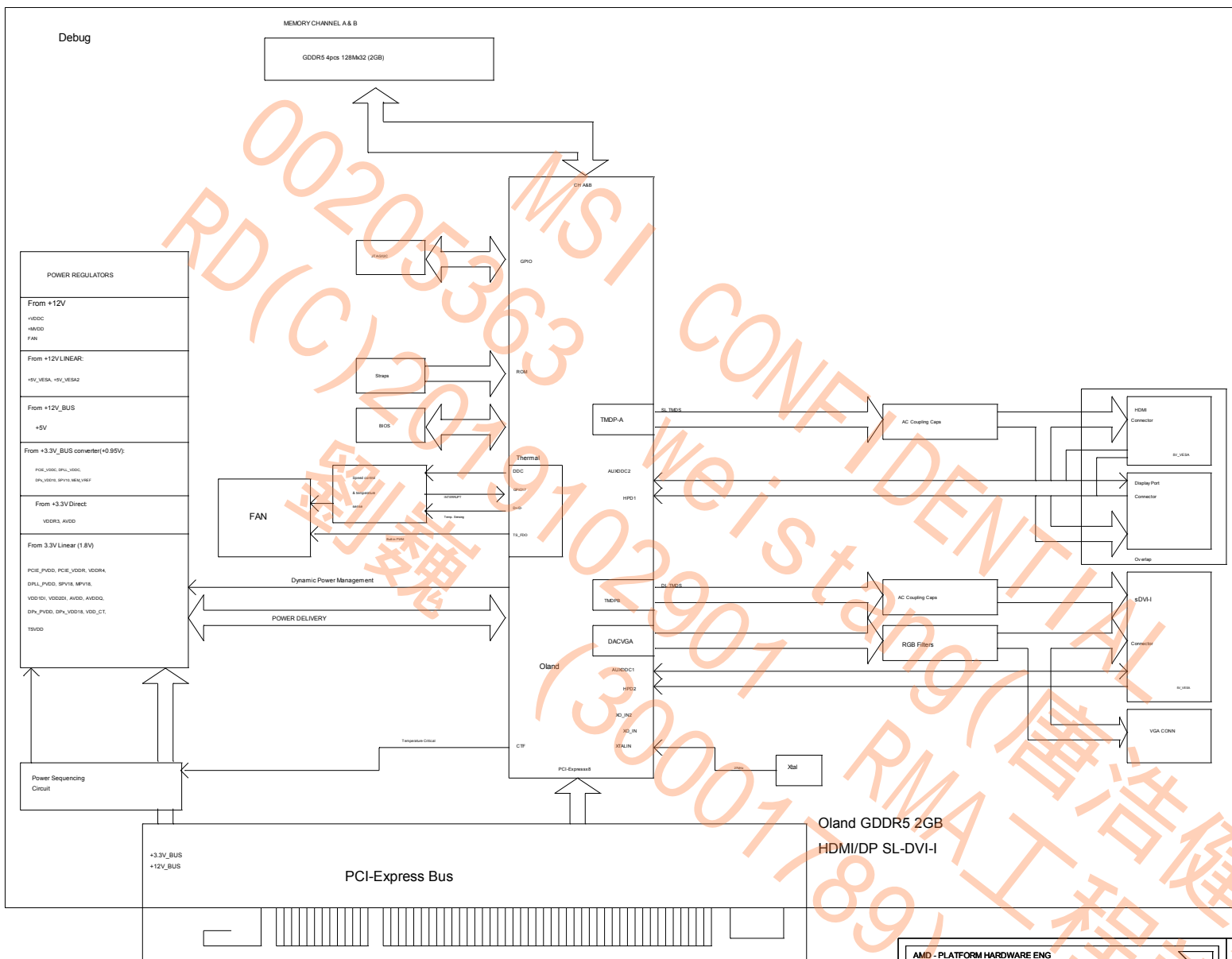
1.8V@0.5A


3.3V@60mA

3.3V_BUS
3A

| | |
|--|----------|
| AMD - PLATFORM HARDWARE ENG #48, No. 1387, ZHANGDONG ROAD SHANGHAI, CHINA 201203 | |
| SHEET: GPIO DDC HPD map | |
| DATE: Tue Sep 22 06:32:59 2015 | REV: 2.0 |
| SHEET NUMBER: 18 | OF 20 |
| DOCUMENT NUMBER: 105-C869xx-008 | |
| NOTES: NOTE | |

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| TITLE: Oland G5 2GB VGA/DVI-HDMI/DP |



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| SHEET: BLOCK DIAGRAM | | DATE: Fri Sep 18 08:34:41 2015 | | REV: 2.0 | |
| SHEET NUMBER: 19 | | OF 20 | | TITLE: Oland G5 2GB VGA/sDVI-I-HDMI/DP | |
| DOCUMENT NUMBER: 105-C869rev-008 | | | | | |

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AMD



TITLE:

Oland G6 2GB VGA/6DVI+HDMI/DP

DOCUMENT NUMBER:

105-C889wa-008

DATE:

Tue Sep 22 02:20:17 2015

SHEET NUMBER:

20 OF 20

REV:

2.0

REVISION HISTORY

ENGINEER:

Tony Yang

NOTES:

NOTE

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SCH Rev

PCB Rev

Date

REVISION DESCRIPTION

1.00

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06/19/14

1 Initial release

2.00

000

09/22/15

2 AMD VGA, 4K

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